REMARKS

Claims 17-22 are pending in the application. Claims 17-22 stand rejected as allegedly being anticipated by U.S. Patent No. 6,539,541 to Geva ("Geva"). The drawings stand objected to. Claims 18, 19, and 22 stand rejected as allegedly being indefinite.

In view of the remarks herein, Applicant respectfully traverses the rejections and asks that they be withdrawn. Reconsideration and allowance are respectfully requested.

I. The Objection to the Drawings

Applicant is submitting formal drawings with this response, and believes that the objection is now moot.

II. The Rejections under 35 U.S.C. 112

Applicant has amended claim 17 to provide proper antecedent basis for claims 18, 19, and 22, and believes that the rejection is now moot.

III. The Rejections under 35 U.S.C. 102(e)

Applicant notes that Geva is directed to a method of constructing and unrolling speculatively counted loops (see the Abstract of Geva). A loop is counted if the number of iterations that the loop will execute is determined once execution reaches the loop (see column 1, lines 26-28 of Geva). A speculatively counted loop satisfies all the requirements of a counted loop except for the characteristic that a speculatively

counted loop has a loop upper bound that has not been proven to be loop invariant. See column 9, lines 53-56 of Geva. Loop unrolling is described, e.g., in column 8, lines 1-15.

Thus, Geva is directed to a method for more efficiently processing loop structures, and includes no teaching specific to image processing. Applicant notes that FIG. 1 includes a camera 128, and that a person skilled in the art would understand that system 100 is configured to perform some image processing. However, claims 17-22 describe a particular apparatus, where image processing may be performed using the features of the apparatus of claims 17-22.

The office action appears to disregard particular features of claims 17-22 including functional language, for example, that the circuit of claim 17 "stores first states of said image processing elements at a time of a specified image processing result." However, functional limitations may not be disregarded. Applicant directs the Examiner's attention to MPEP 2173.05(g), which states that "There is nothing inherently wrong with defining some part of an invention in functional terms." "A functional limitation must be evaluated and considered, just like any other limitation of the claim..." The Federal Circuit has recently affirmed that functional limitations are now entitled to patentable weight. "A patent applicant is free to recite features of an apparatus either structurally or

functionally." *In re Schreiber*, 128 F.3d 1473, 1478, 44 USPQ.2d 1429, 1432 (Fed. Cir. 1997).

The example at the end of MPEP 2173.05(g) outlines the acceptance of functional limitations and their patentability. The MPEP cites *In re Venezia*, 530 F.2d 956, 189 USPQ 149 (CCPA 1976), in which a claim directed to a kit of component parts capable of being assembled included limitations such as "members adapted to be positioned," and found that the functional limitations serve to precisely define present structural attributes of interrelated component parts of the claimed assembly.

Thus, the office action needs to point to some teaching or suggestion in Geva that elements of FIG. 1 are configured as outlined in the claims. The sections below outline the deficiencies of the office action in this regard.

Claim 17

The office action cites Figures 1, 4, and 5 as allegedly teaching the features of claim 17.

Applicant finds no teaching or suggestion of the features of claim 17 in Geva. Specifically, Geva neither teaches nor suggests the following features of claim 17: (a) a plurality of image processing elements; (b) a circuit that stores first states of said image processing elements at a time of a

specified image processing result; and (c) an early exit circuit that determines a completion of a calculation based on comparing current states with said first states.

(a) A plurality of image processing elements

The office action equates element 100 of FIG. 1 with the "plurality of image processing elements." However, element 100 of FIG. 1 refers to the entire computer system. The office action fails to identify a single image processing element, let alone a plurality of image processing elements.

(b) a circuit that stores first states of said image processing elements at a time of a specified image processing result

The office action appears to equate the counting variable "n" of FIG. 4 with "first states of said image processing elements at a time of a specified image processing result. However, FIGS. 4A, 4B, and 4C illustrate three different versions of a loop. The variable "n" merely designates the number of iterations of the loop being executed. The variable "n" does not represent any state of an image processing element, let alone "first states of said image processing elements at a time of a specified image processing result."

(c) an early exit circuit that determines a completion of a calculation based on comparing current states with said first states, wherein the current states of said image processing

elements are characterized by one or more characteristics of said image processing elements at a current time

The office action alleges that FIG. 4 teaches this element, and equates current states with the indicia "i" and first states with the counting variable "n." Again, FIGS. 4A to 4C show three different versions of a loop. There is no teaching or suggestion in Geva of a circuit that compares current states of image processing elements to first states of the image processing elements.

Claim 18

The office action appears to equate processor 102 with the image processing elements in the rejection of claim 18. However, there is no teaching or suggestion in Geva that processor 102 include a plurality of image processing elements, or that characteristics of current states of the image processing elements include arithmetic states of the image processing elements.

Claim 19

Again, Applicant finds no teaching or suggestion that system 100 include image processing elements including accumulators, or that characteristics of current states of the image processing elements include sign bits of the accumulators.

Claim 22

Applicant finds no teaching or suggestion in Geva that characteristics of current states of image processing elements include states of groups of the image processing elements.

Claims 18-22

Claims 18-22 are further patentable for at least the additional reason that they depend from claim 17.

For at least the above reasons, claims 17-22 are patentable over Geva.

CONCLUSION

For at least the reasons outlined above, claims 17-22 are in condition for allowance. If the Examiner has any questions regarding this response, the Examiner is invited to call the undersigned at (858) 678-5070.

Enclosed is a $110.00 check for the Petition for Extension of Time fee for the drawings being submitted herewith.

Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 12/08/03

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Attachments: Formal Drawings (5 sheets)
Information Disclosure Statment

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